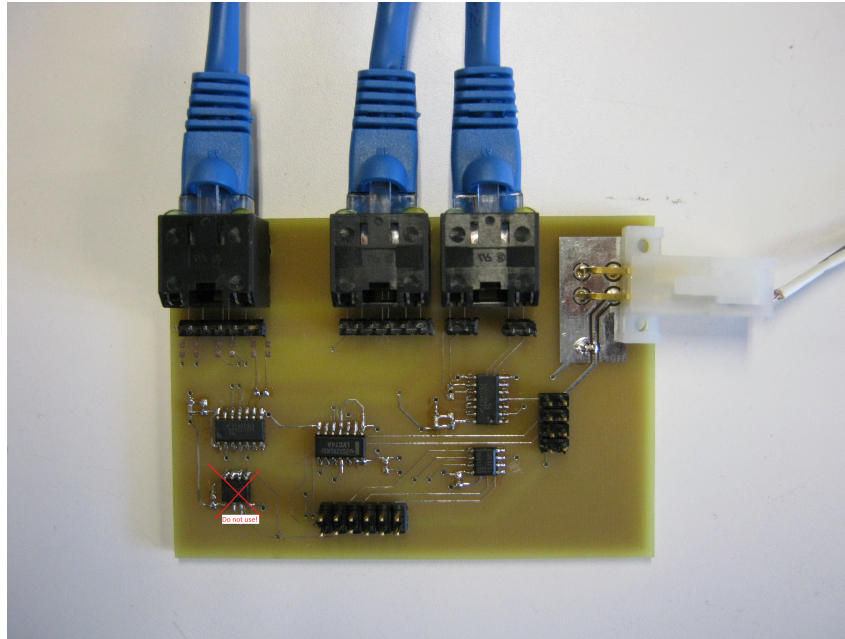


## Tuning a Quad Module using DeMux Boards

### 1. Power

- A) Power quad module, each chip needs 600mA and the mux need 100 mA (2.5A min).
- B) Power two (2) demux boards with 3.3V each, needs 55mA each



### 2. Connectors

- A) Connect RJ45 DO1 output from flex into RJ45 connector on demux board (left contains single DO1 input)
- B) Connect output 1 (middle RJ45 in fig. 1) from demux board into input 1 of Burn-in-Card
- C) Connect output 2 (rightmost RJ45 in fig. 1) from demux board into input 2 of Burn-in-Card
- D) Connect RJ45 DO2 output from flex into RJ45 connector on demux board
- E) Connect output 1 (middle RJ45 in fig. 1) from demux board into input 3 of Burn-in-Card
- F) Connect output 2 (rightmost RJ45 in fig. 1) from demux board into input 4 of Burn-in-Card

### 3. Structure

- A) DO1 and DO2 contain muxed data from quad module
- B) Output 1 (on demux) contains CMD and CLK that bypasses entire demuxboard and is fed directly into quad module
- C) Output 2 uses CLK (same CLK as input 1,2,3,4) for demuxing on flip-flop

Readout Configuration				
Input Port:	Port 1 (BIC + SCA)	Port 2 (BIC)	Port 3 (BIC)	Port 4 (BIC)
Input Divider:	1:4 (40 MBit/s)	1:4 (40 MBit/s)	1:4 (40 MBit/s)	1:4 (40 MBit/s)
Readout Channel:	Channel 0	Channel 1	Channel 2	Channel 3
Readout Channel Input:	1 (direct)	2 (direct)	3 (direct)	4 (direct)
Read Chip Index:	Auto -> Save	Auto -> Save	Auto -> Save	Auto -> Save

### 4. STControl settings

- A) Set configuration as shown in fig. 2
  - i. Auto-Save is recommended to be able to identify GA with FE channel
  - ii. 80MBit/s and 160MBit/s do not work, only use 40MBit/s
- B) Enable Manchester Encoding, clock phase: 1
- C) Change CLK0 to zero (0) for all chips under "FE Global"
- D) Initialize and configure all modules, check "Read chip index" from fig.2 and it should have changed to static values (e.g. FE0 Channel 0, etc....)
5. Run analog and digital tests
  - A) Analog test
    - i. Change "1/Frequency" to 8000, change to steps: 8 and steps\_8
    - ii. Scan takes about 2 minutes to complete
  - B) Digital test
    - i. Change "1/Frequency" to 8000, change to steps: 32 and steps\_32
    - ii. Scan takes about 2 minutes to complete
  - C) Verify that chips are in working condition
6. Run Threshold Scan
  - A) Change "Vthin\_AltFine" in "FE Global" to 130 for all four chips, change "Vthin\_AltCourse" to 0
  - B) Change "1/Frequency" to 8000, change to steps: 8 and steps\_8
  - C) Change "#steps" in loop 0 to 26 (51 steps preferably)
  - D) Scan takes about 10 minutes to complete (20 minutes for 51)
  - E) Results
    - i. "PLOTSCURVE\_MEAN" shows distribution of threshold for pixels in chip, aim for 3000e at first
    - ii. If mean is less than 2900 increase "Vthin\_AltFine" by 10, if mean is greater than 3100 decrease "Vthin\_AltFine" by 10
  - F) Repeat steps B-E until all chips have mean between 2900-3100
7. Noise
  - A) "Plot occupancy" will show you the result at every step in the threshold scan
  - B) Go through each step per chip and identify noisy columns, then disable them
8. Run TDAC\_TUNE
  - A) Change "1/Frequency" to 8000, change to steps: 8 and steps\_8
  - B) Scan takes about 1 minute to complete
  - C) Results
    - i. "TDAC\_OCC" should have a mean of 200
    - ii. "TDAC\_T" should have a mean of 15
  - D) Save cfg as new file (in case tuning failed)
9. Run Threshold Scan
  - A) Repeat steps 6B-6D
  - B) Mean should remain between 2900-3100 but sigma should be significantly smaller (about 50)
10. More tuning
  - A) If default setting of scan is "1/Frequency" = 4000, and mask steps: 3 steps\_3, Change "1/Frequency" to 8000, change to steps: 8 and steps\_8
  - B) If default setting of scan is "1/Frequency" = 8000, and mask steps: 6 steps\_6, Change "1/Frequency" to 8000, change to steps: 32 and steps\_32